OBLON
SPIVAK

ATTORNEYS AT LAW

1940 DUKE STREET
ALEXANDRIA, VIRGINIA 22314
USA

(703) 413-3000
(703) 413-2220 FACSIMILE

OBLONPAT@OBLON.COM

PATENT, TRADEMARK AND COPYRIGHT LAW
AND RELATED FEDERAL AND ITC LITIGATION

WWW.OBLON.COM

FACSIMILE

PLEASE CALL US AT (703) 413-3000 IF THE MESSAGE YOU RECEIVE IS INCOMPLETE OR NOT LEGIBLE

TO	Shamim Ahmed (NAME)	April 5, 2010 (DATE)	
	USPTO (COMPANY/FIRM)	571-273-1457 (FAX #)	
	NUMBER OF PAGES INCLUDING COVER: _____	CONFIRM FAX: ■ YES ☐ NO	
FROM	Pranay Pattani (NAME)	282143US2PCT (OUR REFERENCE)	
	703-412-4533 (DIRECT PHONE #)	10/560,528 (YOUR REFERENCE)	

MESSAGE

Agenda for personal interview scheduled April 5, 2010 at 3 pm.

DOCKET NO: 282143US2PCT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
MASASHI GOTOH, ET AL.	: EXAMINER: AHMED, SHAMIM
SERIAL NO: 10/560,528	:
FILED: DECEMBER 13, 2005	: GROUP ART UNIT: 1792
FOR: METHOD OF MANUFACTURING ELECTRONIC PART AND ELECTRONIC PART	:

INTERVIEW AGENDA

Dear Examiner Ahmed:

Attached is an agenda for the phone interview scheduled April 5, 2010 at 3 pm. Should you have any questions prior to the interview, please call me at (703) 412-4533.

Pranay Pattani

DO NOT ENTER
FOR INTERVIEW PURPOSES ONLY

IN THE CLAIMS

Claim 1 (PROPOSED - Currently Amended): A method of manufacturing an electronic part comprising a conductor film, a lower conductor layer, and an insulating member sandwiched between the conductor film and the lower conductor layer, for connecting the conductor film and the lower conductor layer by conductor portions and growing metal plating on the conductor portions and the conductor film, the method comprising:

forming a plurality of opening holes, each having said lower conductor layer as bottoms, through the conductor film and the insulating member from said conductor film side,

growing metal plating layers, as conductor portions from each of the bottoms of said opening holes, from said lower conductor layer as an electrode,

growing metal plating layers on the upper surfaces of said conductor film and said conductor portions with said conductor film and said conductor portions as electrodes after said conductor portions are formed in the respective plurality of opening holes by growing said metal plating layers so as to contact said metal plating layers with said conductor film, and to increase area for growing said metal plating layers ~~and reduce~~ when naturally changing current density per unit in said metal plating layers, so as to lower growing speed of said metal plating layers, to thereby form said conductor portions in said opening holes, and forming a thickness enough to form an upper conductor layer.

Claim 2 (PROPOSED - Currently Amended): A method of manufacturing an electronic part in which on the upper surface of an insulating member covering a lower

DO NOT ENTER
FOR INTERVIEW PURPOSES ONLY

conductor layer, conductor portions connected from said lower conductor layer are exposed, the method comprising:

forming conductor film on the upper surface of said insulating member and protective film formed on a part of the upper surface of said insulating member and protective film in a thickness direction, and thereafter forming a plurality of opening holes of which bottom is formed by said lower conductor layer, through said protective film and said conductor film,

growing metal plating layers, as said conductor portions from the bottoms of said plurality of opening holes with said lower conductor layer as an electrode, and

growing metal plating on the upper surfaces of said conductor film and said conductor portions with said exposed conductor film and said conductor portions on which protective film is not formed as electrodes, to thereby form a thickness enough to form an upper conductor layer after said conductor portions are formed to the substantial same height in the respective plurality of opening holes by growing said metal plating layers so as to contact said metal plating layers with said conductor film, and to increase area for growing said metal plating layers ~~and reduce~~ when naturally changing current density per unit in said metal plating layers, so as to lower growing speed of said metal plating layers, to thereby form said conductor portions in said opening holes.

DO NOT ENTER
FOR INTERVIEW PURPOSES ONLY

POINTS TO DISCUSS

1. The Office Action states that Tsai teaches "to increase area for growing said metal plating layers and reduce current density per unit in said metal plating layers, so as to lower growing speed of said metal plating layer."

However, Tsai is directed to a "Damascene process" and a "CMP Process." Specifically, at the time of stating the metal growing by electrolytic plating, ***density of current applied*** thereto 15 set to lower level to suppress the growing speed of the metal, so that the metal growing on side wall or opening area of the via hole, ***is lowered*** to obtain so-called void-free copper layer. That is, the current density of current and the entire current value applied to deposit the cupper layer is intentionally and actually controlled.

On the contrary, in an exemplary aspect in the present invention, the entire value of current applied onto the lower conductor layer ***is maintained at constant*** value but the current density thereof ***naturally changes*** because the metal plating layer grows to contact the conductor film and as the result the area on which the current used for metal growing enlarges.

2. Claim language to clarify the above difference.

OBLON SPIVAK

ATTORNEYS AT LAW

1940 DUKE STREET
ALEXANDRIA, VIRGINIA 22314
USA

(703) 413-3000
(703) 413-2220 FACSIMILE

OBLONPAT@OBLON.COM

PATENT, TRADEMARK AND COPYRIGHT LAW AND RELATED FEDERAL AND ITC LITIGATION

WWW.OBLON.COM

FACSIMILE

PLEASE CALL US AT (703) 413-3000 IF THE MESSAGE YOU RECEIVE IS INCOMPLETE OR NOT LEGIBLE

TO	Shamim Ahmed (NAME)	April 5, 2010 (DATE)	
	USPTO (COMPANY/FIRM)	571-273-1457 (FAX #)	
	NUMBER OF PAGES INCLUDING COVER:	CONFIRM FAX: ■ YES ☐ NO	
FROM	Pranay Pattani (NAME)	282143US2PCT (OUR REFERENCE)	
	703-412-4533 (DIRECT PHONE #)	10/560,528 (YOUR REFERENCE)	

MESSAGE

Agenda for personal interview scheduled April 5, 2010 at 3 pm.

DOCKET NO: 282143US2PCT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
MASASHI GOTOH, ET AL.	: EXAMINER: AHMED, SHAMIM
SERIAL NO: 10/560,528	:
FILED: DECEMBER 13, 2005	: GROUP ART UNIT: 1792
FOR: METHOD OF MANUFACTURING ELECTRONIC PART AND ELECTRONIC PART	:

INTERVIEW AGENDA

Dear Examiner Ahmed:

Attached is an agenda for the phone interview scheduled April 5, 2010 at 3 pm. Should you have any questions prior to the interview, please call me at (703) 412-4533.

Pranay Pattani

DO NOT ENTER
FOR INTERVIEW PURPOSES ONLY

IN THE CLAIMS

Claim 1 (PROPOSED - Currently Amended): A method of manufacturing an electronic part comprising a conductor film, a lower conductor layer, and an insulating member sandwiched between the conductor film and the lower conductor layer, for connecting the conductor film and the lower conductor layer by conductor portions and growing metal plating on the conductor portions and the conductor film, the method comprising:

forming a plurality of opening holes, each having said lower conductor layer as bottoms, through the conductor film and the insulating member from said conductor film side,

growing metal plating layers, as conductor portions from each of the bottoms of said opening holes, from said lower conductor layer as an electrode,

growing metal plating layers on the upper surfaces of said conductor film and said conductor portions with said conductor film and said conductor portions as electrodes after said conductor portions are formed in the respective plurality of opening holes by growing said metal plating layers so as to contact said metal plating layers with said conductor film, and to increase area for growing said metal plating layers ~~and reduce~~ when naturally changing current density per unit in said metal plating layers, so as to lower growing speed of said metal plating layers, to thereby form said conductor portions in said opening holes, and forming a thickness enough to form an upper conductor layer.

Claim 2 (PROPOSED - Currently Amended): A method of manufacturing an electronic part in which on the upper surface of an insulating member covering a lower

DO NOT ENTER
FOR INTERVIEW PURPOSES ONLY

conductor layer, conductor portions connected from said lower conductor layer are exposed, the method comprising:

forming conductor film on the upper surface of said insulating member and protective film formed on a part of the upper surface of said insulating member and protective film in a thickness direction, and thereafter forming a plurality of opening holes of which bottom is formed by said lower conductor layer, through said protective film and said conductor film,

growing metal plating layers, as said conductor portions from the bottoms of said plurality of opening holes with said lower conductor layer as an electrode, and

growing metal plating on the upper surfaces of said conductor film and said conductor portions with said exposed conductor film and said conductor portions on which protective film is not formed as electrodes, to thereby form a thickness enough to form an upper conductor layer after said conductor portions are formed to the substantial same height in the respective plurality of opening holes by growing said metal plating layers so as to contact said metal plating layers with said conductor film, and to increase area for growing said metal plating layers ~~and reduce~~ when naturally changing current density per unit in said metal plating layers, so as to lower growing speed of said metal plating layers, to thereby form said conductor portions in said opening holes.

DO NOT ENTER
FOR INTERVIEW PURPOSES ONLY

POINTS TO DISCUSS

1. The Office Action states that Tsai teaches "to increase area for growing said metal plating layers and reduce current density per unit in said metal plating layers, so as to lower growing speed of said metal plating layer."

However, Tsai is directed to a "Damascene process" and a "CMP Process." Specifically, at the time of stating the metal growing by electrolytic plating, ***density of current applied*** thereto 15 set to lower level to suppress the growing speed of the metal, so that the metal growing on side wall or opening area of the via hole, ***is lowered*** to obtain so-called void-free copper layer. That is, the current density of current and the entire current value applied to deposit the cupper layer is intentionally and actually controlled.

On the contrary, in an exemplary aspect in the present invention, the entire value of current applied onto the lower conductor layer ***is maintained at constant*** value but the current density thereof ***naturally changes*** because the metal plating layer grows to contact the conductor film and as the result the area on which the current used for metal growing enlarges.

2. Claim language to clarify the above difference.